REMARKS

Claims 1-31 are currently pending in the subject application, and are presently under consideration. Claims 1-18 are rejected. Claims 1, 3, 6, 10, 11, 16, and 17 have been amended. Claims 2, 8, 9, 12, 13, and 18 have been cancelled. New claims 19-31 have been added. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. Rejection of Claims 1-4 and 11-14 Under 35 U.S.C. §102(e)

Claims 1-4 and 11-14 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Publication No. 2002/0110134 to Gracon, et al. ("Gracon"). Claims 1, 3, and 11 have been amended. Claims 2, 12, and 13 have been cancelled. Withdrawal of this rejection is respectfully requested for at least the following reasons.

Amended claim 1 recites routing a data stream through a delay device and delaying selected data of the data stream in said network by storing the selected data in memory buffers for a fixed delay amount to control the data rate to increase latency of the network. Gracon teaches a packet scheduler that accepts packet identifiers from a packet manager, processes the received packet identifiers, and informs the packet manager to output packets at designated time slots or drop certain packets if congestion occurs (paragraph 10). Accordingly, the packet scheduler taught by Gracon is not a delay device, as recited in amended claim 1. The packet scheduler of Gracon assigns priority levels to packets and routes them according to those priority levels (see, e.g., paragraphs 22, 26, and 27). Assuming *arguendo* that there are routing delays in the system of Gracon, any delay in routing packets is as a result of the packets being of a lower priority, and not for storing the selected data in memory buffers for a fixed delay amount to control the data rate to increase latency of the network, as recited in amended claim 1. Also, assuming *arguendo* that there are routing delays in the system of Gracon, Gracon does not teach delaying selected data in the network by a fixed delay amount, as recited in amended claim 1, as packets of varying priority will be sent at various times in the system of Gracon. Additionally, the system of Gracon does not teach controlling the data rate to increase latency of the network

by storing the selected data in memory buffers, as recited in amended claim 1. Instead, the system of Gracon employs a congestion manager that performs congestion tests on received packets and drops the packets if they fail any of the tests (paragraph 46). In so doing, the system of Gracon is actually decreasing latency of a network by transmitting communication packets of higher priority and dropping packets that fail congestion tests. Accordingly, Gracon does not anticipate amended claim 1. Withdrawal of the rejection of claim 1, as well as claims 3-5 which depend therefrom, is respectfully requested.

Amended claim 3 recites that the fixed delay amount is stored in a configuration table, and said delay device consults the configuration table to determine when to release the selected data from the memory buffers. Gracon teaches congestion parameters in a congestion table that are determinative of whether the congestion manager should drop a packet or send it to the scheduler (paragraph 46). The congestion parameters are not indicative of when to release selected data from memory buffers, as recited in amended claim 3. Therefore, Gracon does not teach that the fixed delay amount is stored in a configuration table, and said delay device consults the configuration table to determine when to release the selected data from the memory buffers, as recited in amended claim 3. Accordingly, Gracon does not anticipate amended claim 3. Withdrawal of the rejection of claim 3 is respectfully requested.

Amended claim 11 recites routing a data stream through a delay device and delaying data in a network by storing the data in memory buffers for a fixed delay amount to control the data rate to increase latency of the network, the data being delayed by a varying delay amount that is slowly adjusted over time by passing the data rate through a low pass filter. Regarding a delay device and delaying data in a network by storing the data in memory buffers for a fixed delay amount to control the data rate to increase latency of the network, amended claim 11 should be allowable for at least the reasons discussed above regarding amended claim 1. In addition, the Office Action dated January 11, 2005 (page 3, citing paragraph 45), asserts that Gracon teaches a low-pass filter, as recited in claim 11. Representative for Applicant respectfully disagrees. The low-pass filter discussed in Gracon is used to calculate an average queue size, such that the average queue size is compared with a threshold value to determine if a packet should be

dropped (paragraph 45). Gracon does not, however, teach that the data is delayed by a varying delay amount that is slowly adjusted over time by passing the data rate through a low pass filter, as recited in amended claim 11. Accordingly, Gracon does not anticipate amended claim 11. Withdrawal of the rejection of claim 11, as well as claims 14 and 15 which depend therefrom, is respectfully requested.

For the reasons described above, claims 1, 3, 4, 11, and 14 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

II. Rejection of Claims 5-10 and 15-18 Under 35 U.S.C. §103(a)

Claims 5-10 and 15-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gracon in view of U.S. Patent No. 6,732,168 to Bearden, et al. ("Bearden"). Claims 6, 10, and 16 have been amended. Claims 8, 9, 12, 13, and 18 have been cancelled. Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claims 5 and 15, which depend from amended claims 1 and 11, respectively, recite that the network includes at least one client processor, at least one server processor, at least one network router, and a delay processor. Amended claim 1 recites routing a data stream through a delay device and delaying selected data of the data stream in said by storing the selected data in memory buffers for a fixed delay amount to control the data rate to increase latency of the network. As described above regarding claim 1, the packet scheduler taught by Gracon is not a delay device, as recited in amended claim 1, and Gracon does not teach delaying selected data in the network by a fixed delay amount, as further recited in amended claim 1. Additionally, amended claim 11 recites that the data being delayed by a varying delay amount that is slowly adjusted over time by passing the data rate through a low pass filter. As described above regarding claim 11, Gracon does not teach data being delayed by a varying delay amount that is slowly adjusted over time by passing the data rate through a low pass filter, as recited in amended claim 11.

The addition of Bearden does not cure the above cited deficiencies of Gracon to teach or suggest amended claims 1 and 11, from which claims 5 and 15 depend. Bearden teaches a

policy-based network management system realized by policy-based management programs defined by policy packages (Abstract), and is relied upon by the Office Action dated January 11, 2005, (page 4) to teach a network that includes a client processor, at least one server processor, and at least one network router. However, neither Gracon nor Bearden, individually or in combination, teach or suggest amended claims 1 and 11, from which claims 5 and 15 depend. Therefore, claims 5 and 15 should be allowed over the cited art. Withdrawal of the rejection of claims 5 and 15 is respectfully requested.

Amended claim 6 recites a delay processor for controlling the data rate in a network, the delay processor being operative to store data packets in a plurality of memory buffers for a fixed amount of time and releasing the data packets after the fixed amount of time to increase latency of the network. For the reasons discussed above regarding amended claim 1, Gracon does not teach or suggest a delay processor operative to store data packets in a plurality of memory buffers for a fixed amount of time, as recited in amended claim 6. Also, as discussed above regarding claim 1, the system of Gracon employs a congestion manager that performs congestion tests on received packets and drops the packets if they fail any of the tests (paragraph 46), thus decreasing latency of a network by transmitting communication packets of higher priority and dropping packets that fail congestion tests. Therefore, Gracon does not teach or suggest controlling the data rate in a network by storing data packets in a plurality of memory buffers for a fixed amount of time and releasing the data packets after the fixed amount of time to increase latency of the network, as recited in amended claim 6.

The addition of Bearden does not cure the deficiencies of Gracon to teach or suggest amended claim 6. Bearden is relied upon by the Office Action dated January 11, 2005 (page 5) to teach a first processor and a second processor each connected to the network. However, neither Gracon nor Bearden, individually or in combination, teach or suggest a delay processor for controlling the data rate in a network, the delay processor being operative to store data packets in a plurality of memory buffers for a fixed amount of time and releasing the data packets after the fixed amount of time to increase latency of the network, as recited in amended

claim 6. Therefore, amended claim 6 should be allowed over the cited art. Withdrawal of the rejection of claim 6, as well as claim 7 which depends therefrom, is respectfully requested.

Amended claim 10 recites that the fixed amount of time is stored in a configuration table, the delay processor consulting the configuration table to determine when to release the data packets from the memory buffers. For the reasons discussed above regarding amended claim 3, Gracon does not teach or suggest amended claim 10. Also, the addition of Bearden does not cure the deficiencies of Gracon to teach or suggest amended claim 10, such that neither Gracon nor Bearden, alone or in combination, teach or suggest that the fixed amount of time is stored in a configuration table, the delay processor consulting the configuration table to determine when to release the data packets from the memory buffers, as recited in amended claim 10. Withdrawal of the rejection of claim 10 is respectfully requested.

Amended claim 16 recites a delay processor for controlling the data rate in a network, the delay processor delaying data in the network by storing the data in memory buffers and releasing the data after a delay, the amount of the delay being variably controlled by the output of the low pass filter, where the low pass filter receives the data rate as an input. For the reasons discussed above regarding amended claim 6, neither Gracon nor Bearden, individually or in combination, teach or suggest a delay processor for controlling the data rate in a network, the delay processor delaying data in the network by storing the data in memory buffers and releasing the data after a delay, the amount of the delay being variably controlled by the output of the low pass filter, where the low pass filter receives the data rate as an input, as recited in amended claim 16. Therefore, claim 16 should be allowed over the cited art. Withdrawal of the rejection of claim 16, as well as claim 17 which depends therefrom, is respectfully requested.

For the reasons described above, claims 5-7 and 15-17 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

III. New Claims 19-31

New Claim 19 depends from amended claim 1 and recites determining the selected data of the data stream by employing a packet selection list that indicates which of the data packets

are to be the delayed selected data. Neither Gracon nor Bearden, individually or in combination, teach or suggest determining the selected data of the data stream by employing a packet selection list that indicates which of the data packets are to be the delayed selected data, as recited in new claim 19. Accordingly, new claim 19 should be patentable over the cited art.

New claim 20 depends from amended claim 1 and recites determining the amount of time the selected data is stored in the memory buffers based on an amount of delay stored in a configuration table. Neither Gracon nor Bearden, individually or in combination, teach or suggest determining the amount of time the selected data is stored in the memory buffers based on an amount of delay stored in a configuration table, as recited in new claim 20. Accordingly, new claim 20 should be patentable over the cited art.

New claim 21 depends from new claim 20 and recites updating the configuration table to change the amount of delay stored in the configuration table upon the delay device receiving a configuration table packet. Neither Gracon nor Bearden, individually or in combination, teach or suggest updating the configuration table to change the amount of delay stored in the configuration table upon the delay device receiving a configuration table packet, as recited in new claim 21. Accordingly, new claim 21 should be patentable over the cited art.

New claim 22 depends from amended claim 1 and recites storing a release time in the memory buffers along with the selected data, the release time corresponding to a time at which the selected data is to be released from the memory buffers. Neither Gracon nor Bearden, individually or in combination, teach or suggest storing a release time in the memory buffers along with the selected data, the release time corresponding to a time at which the selected data is to be released from the memory buffers, as recited in new claim 22. Accordingly, new claim 22 should be patentable over the cited art.

New claim 23 depends from amended claim 6 and recites that the delay processor comprises a packet selection list that indicates which of the data packets are to be delayed through the delay processor. For the reasons described above regarding new claim 19, new claim 23 should be patentable over the cited art.

New claim 24 depends from amended claim 6 and recites that the delay processor comprises a clock circuit and a controller operative to determine the fixed amount of time the data packets are stored in the memory buffers based on an amount of delay stored in a configuration table. For the reasons described above regarding new claim 20, new claim 24 should be patentable over the cited art.

New claim 25 depends from new claim 24 and recites that the controller stores a release time in the memory buffers along with the data packets, the release time corresponding to a time at which the data packets are to be released from the memory buffers by the controller. For the reasons described above regarding new claim 22, new claim 25 should be patentable over the cited art.

New claim 26 depends from amended claim 11 and recites determining which of the data of the data stream to be delayed by employing a packet selection list that indicates which of the data packets are to be the delayed data. For the reasons described above regarding new claim 19, new claim 26 should be patentable over the cited art.

New claim 27 depends from amended claim 11 and recites storing the varying delay amount in a configuration table and determining the amount of time the delayed data is stored in the memory buffers based on the varying delay amount stored in the configuration table. For the reasons described above regarding new claim 20, new claim 27 should be patentable over the cited art.

New claim 28 depends from amended claim 16 and recites storing a release time in the memory buffers along with the delayed data, the release time corresponding to a time at which the delayed data is to be released from the memory buffers. For the reasons described above regarding new claim 22, new claim 28 should be patentable over the cited art.

New claim 29 depends from amended claim 16 and recites that the delay processor comprises a packet selection list that indicates which of the data is to be delayed. For the reasons described above regarding new claim 19, new claim 29 should be patentable over the cited art.

New claim 30 depends from amended claim 16 and recites that the delay processor comprises a clock circuit and a controller operative to determine the amount of time the data is

stored in the memory buffers based on the variably controlled amount of delay being stored in a configuration table. For the reasons described above regarding new claim 20, new claim 30 should be patentable over the cited art.

New claim 31 depends from new claim 30 and recites that the controller stores a release time in the memory buffers along with the data, the release time corresponding to a time at which the data is to be released from the memory buffers by the controller. For the reasons described above regarding new claim 22, new claim 31 should be patentable over the cited art.

CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Please charge any deficiency or credit any overpayment in the fees for this amendment to our Deposit Account No. 20-0090.

Respectfully submitted,

Date 3/31/05

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